AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A pseudo-random number generator comprising:

a linear feedback register including a plurality of registers connected in series, a first logical operation circuit for taking logical operation of output data from the predetermined registers to deliver the result of the logical operation, and a second logical operation circuit for taking logical operation of input data supplied from the outside and output data of said first logical operation circuit to supply any one of said plurality of registers with the result of the logical operation, said linear feedback register generating pseudo-random numbers from said registers; [[and]]

an oscillator for generating a third clock which is unstable in frequency during a first time period immediately following turn-ON of said pseudo-random number generator;

a Pre-SEED generator circuit for supplying, only during the first time period, said linear feedback register with a shift clock which is generated by taking logical operation of said third clock and a fourth clock asynchronous to said third clock and for supplying, only during the first time period, said linear

feedback register with said input data which comprises said fourth clock;

a signal generator for generating [[a]] said shift clock for operating said linear feedback register[[,]] only after the first time period and for generating said input data using a first clock at a constant period and a second clock synchronized to said first clock only after the first time period; and

an access controller that extracts the pseudo-random numbers from said linear feedback register and outputs the pseudo-random numbers.

2. (canceled)

3. (original) The pseudo-random number generator according to claim 1, wherein:

said signal generator delivers said shift clock which is one of said first clock and a clock generated by dividing said first clock, said first clock and said divided clock being switched at predetermined intervals.

4. (currently amended) The pseudo-random number generator according to claim 1, ~~further comprising: an~~ wherein said access controller ~~for reading a random number~~ reads the pseudo-random numbers generated by said linear feedback register at a cycle different from the period of said shift clock.

5. (original) The pseudo-random number generator according to claim 1, further comprising:

a write circuit for providing logical operation of output data from said linear feedback register and arbitrary data entered from the outside,

wherein said linear feedback register rewrites an initial value into said registers with data delivered from said write circuit.

6. (original) The pseudo-random number generator according to claim 1, wherein said linear feedback register comprises a number of registers larger than the number of bits of said random number.